



(11) Publication number : **0 611 129 A2**

## EUROPEAN PATENT APPLICATION

(12)

(21) Application number : **94300900.1**

(51) Int. Cl.<sup>5</sup> : **H01L 21/58**

(22) Date of filing : **08.02.94**

(30) Priority : **08.02.93 US 14481**  
**09.07.93 US 87434**

(43) Date of publication of application :  
**17.08.94 Bulletin 94/33**

(84) Designated Contracting States :  
**DE FR GB IT NL**

(71) Applicant : **GENERAL ELECTRIC COMPANY**  
**1 River Road**  
**Schenectady, NY 12345 (US)**

(72) Inventor : **Fillion, Raymond Albert**  
**31 Chestnut Lane**  
**Schenectady, New York 12309 (US)**  
Inventor : **Wojnarowski, Robert John**  
**1023 Hatlee Road**  
**Ballston Lake, New York 12019 (US)**  
Inventor : **Gdula, Michael**  
**Witter Road,**  
**P O Box 8**  
**Knox, New York 12107-0008 (US)**  
Inventor : **Cole, Herbert Stanley**  
**8 Evergreen Courte**  
**Burnt Hills, New York 12027 (US)**  
Inventor : **Wildi, Eric Joseph**  
**64 Pheasant Ridge**  
**Niskayuna, New York 12309 (US)**  
Inventor : **Daum, Wolfgang**  
**804 DeCamp Avenue**  
**Schenectady, New York 12309 (US)**

(74) Representative : **Lupton, Frederick et al**  
**LONDON PATENT OPERATION,**  
**G.E. TECHNICAL SERVICES Co. INC.,**  
**Essex House,**  
**12/13 Essex Street**  
**London WC2R 3AA (GB)**

(54) **Embedded substrate for integrated circuit modules.**

(57) Substrate material is molded directly to semiconductor chips and other electrical components that are positioned for integrated circuit module fabrication. Chips having contact pads are placed face down on a layer of adhesive supported by a base. A mold form is positioned around the chips. Substrate molding material is added within the mold form, and the substrate molding material is then hardened. A dielectric layer having vias aligned with predetermined ones of the contact pads and having an electrical conductor extending through the vias is situated on the hardened substrate molding material and the faces of the chips. A thermal plug may be affixed to the backside of a chip before substrate molding material is added. A connector frame may be placed on the adhesive layer before substrate molding material is added. A dielectric layer may be placed over the backsides of the chips before the substrate molding material is added to enhance repairability. A portion of the chips and substrate molding material may be removed after the substrate molding material is hardened.

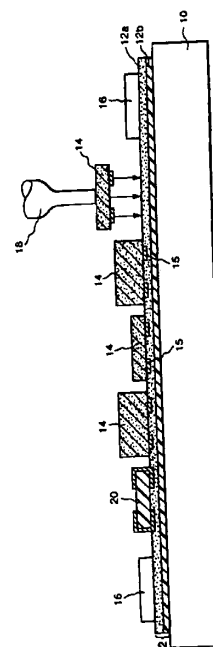


FIG. 1(a)

EP 0 611 129 A2

## BACKGROUND OF THE INVENTION

### Field of the Invention

This invention relates generally to fabrication of substrates for multi-chip modules and other integrated circuit modules, and, more particularly, to fabrication of a substrate for an integrated circuit module by molding material around semiconductor chips, except for chip surfaces containing contact pads.

### Description of the Related Art

Conventional high density interconnect (HDI) processes often use cavities formed into a substrate base for the placement of chips so that the top surfaces of the chips are essentially planar with the surface of the substrate. The substrate is generally a ceramic or a composite structure. The conventional HDI technique for fabricating cavities in the substrate is to mechanically machine or mill out the cavity material with a computer-controlled diamond tooled bit. This time consuming process does not always provide the desired chip cavity depth and can result in cracks which render the substrate unusable.

In the conventional HDI process, chips are placed into cavities on multiple drops of die attach adhesive for mechanical, thermal, and electrical mounting. Chips placed with this process often are displaced during further processing because there are non-uniform surface tension forces at the chip-to-die attach adhesive interface. This displacement reduces precision in chip location, and further processing steps are required to adapt each electrical interconnection to the chip misalignment.

Eichelberger, U.S. Pat. No. 5,091,769, issued Feb. 25, 1992, describes an integrated circuit package formed by placing integrated circuit chips backside down on a substrate, encapsulating the faces and sides of the chips, fabricating vias and interconnections through the encapsulant to the contact pads for testing and burn in procedures, and removing the encapsulant after testing. When chips of differing thicknesses are used in a single multi-chip module (MCM), their pads are not situated in a common plane, so this method requires either that some of the chips be thinned or that the vias be of varying depths. Additionally, this technique involves a step of mechanical grinding for planarizing the surface and the use of an encapsulant material which is removed after testing.

### SUMMARY OF THE INVENTION

Accordingly, an object of the invention is to provide a method for positioning contact pads of a plurality of chips with differing thicknesses on a planar surface without milling chip wells or thinning chips.

Another object of the invention is to provide an easily implemented, high yield and high reliability process for precisely positioning chips in a substrate with improved thermal cooling paths and for providing the chips with electrical connection to external circuitry.

Yet another object of the invention is to provide a method for chip placement and alignment such that the positions of the chip contact pads are precisely aligned.

Briefly, according to a preferred embodiment of the invention, a method of fabricating an integrated circuit module substrate on a base comprises applying an insulative base sheet over the base. At least one chip having contact pads is placed face down on the base sheet including an adhesive. A mold form is positioned around a desired perimeter and surrounds at least one chip. Substrate molding material is added and then hardened within the mold form.

According to another preferred embodiment of the invention, chips having contact pads are disposed on a base sheet with the contact pads in contact with the base sheet. The base sheet is comprised of an adhesive layer on a polymer film layer which is disposed on a base comprised of any convenient structural material. A mold form is disposed on the adhesive layer, surrounding the chips. A polymeric molding material is added to the mold form encapsulating all surfaces of the chips except the surfaces containing the contact pads which are in contact with the adhesive layer, and is hardened. The mold form and the supporting base are removed following the hardening of the molding material and the curing of the adhesive layer. The base sheet then serves as a dielectric layer for a high density interconnect (HDI) structure which is subsequently formed. A plurality of vias are disposed through the base sheet in alignment with predetermined contact pads on the chips. An electrical connection is made to the contact pads through a pattern of electrical conductors which overlies the base sheet. The base sheet and pattern of electrical conductors form an interconnect layer over which one or more additional interconnect layers may be subsequently applied.

In another preferred embodiment of the invention, the aforementioned base sheet comprising the adhesive layer and polymer film layer is removed following the hardening of the molding material. After the top surface of the chips and molding material is cleaned, a polymeric film is bonded to that surface with an adhesive to form the dielectric layer.

In still another preferred embodiment of the invention, the base sheet comprises an adhesive layer only, which is applied directly to the base structure. Following the hardening of the mold material, the supporting base structure is separated from the adhesive layer. A film layer is then bonded to the molded substrate by curing the adhesive layer to form the di-

el ctic layer.

In yet another preferred embodiment of the invention, an inner dielectric layer overlies the backside of the chips prior to the addition of the molding material for providing air gaps and easing repair processes.

According to another preferred embodiment of the invention, a method of fabricating an integrated circuit module substrate comprises placing a plurality of chips having contact pads face down on a vacuum plate and applying a continuous vacuum to the vacuum plate. A mold form is positioned around the chips, and substrate molding material is added within the mold form. The substrate molding material is hardened and separated from the vacuum plate. A dielectric layer is applied over the chips and the substrate molding material. A plurality of vias are formed through the dielectric layer with some of the vias being aligned with predetermined ones of the contact pads. A pattern of electrical conductors is applied through selected ones of the plurality of vias in the dielectric layer.

According to yet another embodiment of the invention, a plastic molded substrate is thinned using a mechanical grinding machine, thus resulting in a module having lower weight and less volume. A plurality of such thinned substrates can be bonded and interconnected in a stack assembly.

#### BRIEF DESCRIPTION OF THE DRAWINGS

The features of the invention believed to be novel are set forth with particularity in the appended claims. The invention itself, however, both as to organization and method of operation, together with further objects and advantages thereof, may best be understood by reference to the following description taken in conjunction with the accompanying drawings, where like numerals represent like components, in which:

**FIG. 1(a)** is a sectional side view of chips placed face side down on an adhesive coated film layer, which may comprise a portion of an interconnect layer in the completed module;

**FIG. 1(b)** is a view similar to that of FIG. 1(a), further showing a mold form situated around the chips and containing molding material;

**FIG. 1(c)** is a view similar to that of FIG. 1(b), further showing embedded chips in substrate molding material after the mold form has been removed;

**FIG. 1(d)** is a view similar to that of FIG. 1(c), further showing vias and electrical connections in the adhesive coated film layer;

**FIG. 1(e)** is a view similar to that of FIG. 1(d), further showing interconnect layers;

**FIG. 2(a)** is a view similar to that of FIG. 1(c), after removal of the adhesive coated film which, in this

embodiment, is sacrificial rather than a portion of an interconnect layer;

**FIG. 2(b)** is a view similar to that of FIG. 2(a), further showing another adhesive coated polymer film on the chip and hardened substrate material;

**FIG. 3(a)** is a sectional side view of chips placed face side down on an adhesive layer supported by a base;

**FIG. 3(b)** is a view similar to that of FIG. 3(a), further showing a mold form situated around the chips and containing molding material;

**FIG. 3(c)** is a view similar to that of FIG. 3(b), further showing the embedded chips in the substrate molding material which has been removed from the mold form, has had the base removed, and has been flipped over with the adhesive layer intact on the surface of the chips and the molded substrate;

**FIG. 3(d)** is a view similar to FIG. 3(c), further showing a polymer film applied to the adhesive layer.

**FIG. 4(a)** is a view similar to that of FIG. 1(a), showing an inner dielectric layer over the chips and the adhesive coated film layer;

**FIG. 4(b)** is a view similar to that of FIG. 4(a), further showing a mold form situated around the chips and containing a substrate molding material;

**FIG. 4(c)** is a view similar to that of FIG. 4(a), further showing an electrically conductive strip positioned between the inner dielectric layer and the chip/substrate surface;

**FIG. 4(d)** is a top view of the embodiment shown in FIG. 4(c);

**FIG. 4(e)** is a view similar to that of FIG. 4(c), further showing the chips, the adhesive coated film layer, the inner dielectric layer, and the electrically conductive strip after the molding material has been formed, as well as interconnections in the adhesive coated film layer through vias extending to a contact pad and the electrically conductive strip;

**FIG. 5(a)** is a view similar to that of FIG. 1(a), further including thermal plugs situated on passive backsides of the chips for enhanced heat removal;

**FIG. 5(b)** is a view similar to that of FIG. 5(a), further showing a mold form situated around the chips and thermal plugs containing a molding material;

**FIG. 6(a)** is a view similar to that of FIG. 1(d), further showing a perimeter array of interconnect pins extending through the surface of the substrate molding material opposite the surface to which the chips are attached;

**FIG. 6(b)** is a view similar to that of FIG. 1(d), further showing a perimeter array of interconnect pins extending through a side of the substrate

molding material;

**FIG. 7(a)** is a sectional side view of chips face side down on a base comprising a vacuum plate;

**FIG. 7(b)** is a view similar to that of **FIG. 7(a)**, further showing a mold form situated around the chips and containing molding material;

**FIG. 7(c)** is a view similar to that of **7(b)**, further showing embedded chips in substrate molding material after the mold form has been removed;

**FIG. 7(d)** is a sectional side view of chips face side up on a base comprising a rigid vacuum plate and a compliant vacuum plate for subsequent lowering onto the rigid vacuum plate;

**FIG. 7(e)** is a view similar to that of **FIG. 7(d)**, further showing the compliant vacuum plate in contact with the chips;

**FIG. 7(f)** is a view similar to that of **FIG. 7(e)**, showing the compliant vacuum plate and chips after the removal of the rigid vacuum plate;

**FIG. 8(a)** is a view similar to that of a portion of **FIG. 1(b)**, further showing a grinding fixture for reducing substrate and chip thicknesses;

**FIG. 8(b)** is a view similar to that of **FIG. 8(a)**, showing the chips and substrate after a portion has been removed;

**FIG. 8(c)** is a view similar to that of **FIG. 8(b)**, further showing interconnect layers over the chips;

**FIG. 8(d)** is a view showing a stack of thinned chips having interconnect layers with edge contacts; and

**FIG. 8(e)** is a view showing a stack of thinned chips interconnected by substrate pins.

#### DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT OF THE INVENTION

**FIG. 1(a)** is a sectional side view of chips, represented by a capacitor 20 and semiconductor chips 14, placed face side down on a base sheet 12 supported by a base 10. Base sheet 12 can be comprised of a film layer 12b, such as Kapton polyimide (Kapton is a trademark of E.I. duPont de Nemours and Co.), coated with a contact adhesive layer 12a, such as Ultem polyetherimide resin (Ultem is a registered trademark of General Electric Company, Pittsfield, MA) or an epoxy/polyimide copolymer blend such as that disclosed in commonly assigned Wojnarowski et al., U.S. Pat. No. 5,108,825, issued Apr. 28, 1992, which is herein incorporated by reference. Solvent die attach may be used, as described in US-A-5,225,023. The phrase "face side down" means that contact pads 15 are in contact with adhesive layer 12a. Base 10 may comprise any structural material, such as, for example, plastic, ceramic, or metal.

A chip may comprise any electrical circuit component, including semiconductor chips, such as integrated circuits (ICs), and discrete devices, such as, for example, capacitors, resistors, inductors, and transduc-

ers. Chips 14 or 20, which need not have the same thickness, may be placed in contact with adhesive layer 12a in any conventional manner. In one embodiment, a pick-and-place machine 18 (partially shown) is used. In another embodiment, chips are placed precisely on a temporary surface such as wax or a film having low contact adhesion, such as a wafer membrane of the types fabricated by Nitto Co. (known as "Nitto Tape") and Semiconductor Equipment Corp. (known as "Blue Membrane"), and then the chips, while still attached to the temporary surface, are placed face down on base sheet 12. The use of a temporary surface is most effective when the chips have similar thicknesses.

Base sheet 12, comprised of adhesive layer 12a and polymer film layer 12b, may be used as the first dielectric layer for an HDI structure which typically comprises a thermoplastic or thermoset adhesive applied to a fully cured polymeric film. Alternatively, base sheet 12 may be a sacrificial layer which is removed after molding, as further discussed with respect to **FIGs. 2(a)** and **2(b)**. If the base sheet is used as a first dielectric layer, then preferably both the adhesive and polymer film layers are laser ablatable at wavelengths of 350-370 nm.

In a preferred embodiment, an optional sheet frame 16 is used to keep base sheet 12 flat on the surface of base 10. The frame is typically comprised of molybdenum, titanium, or stainless steel, but may comprise any appropriate structural material. After chip attachment, procedures such as palladium/chloride seed plating, sputtering, and vapor deposition may be used to cover the chips with electrically conductive material as disclosed in commonly assigned Wojnarowski et al., U.S. Pat. No. 5,151,776, issued Sep. 29, 1992, which is herein incorporated by reference.

**FIG. 1(b)** is a sectional side view of the apparatus of **FIG. 1(a)**, further showing a mold form 22 situated around the chips and filled with a substrate molding material 24. Mold form 22 can comprise any appropriate structural material including, for example, plastic or metal and can either remain with the molded substrate during further processing or be removed after preparing the mold. A removable mold form can be either sacrificial or reusable. If the mold form is reusable, it is useful to spray on a release agent (not shown), such as Teflon polytetrafluoroethylene (Teflon is a trademark of E.I. duPont de Nemours and Co.), silicone, or a no-stick vegetable oil before filling the mold form with the molding material.

Potential substrate molding materials include, but are not limited to, aliphatic and aromatic polymers including thermoplastic and thermoset type polymers and blends of various polymers such as Ultem polyetherimide resin, acrylates, polyurethanes, Teflon polytetrafluoroethylene, polyoxies, benzocyclobuten (BCB), polyimides, or other polymers. One im-

important consideration when selecting a molding material is that it must be able to withstand subsequent processing steps and end use environment.

The molding material will likely include therein filler material in a configuration of particles, fibers, screens, mats, or plates. The type and amount of filler material can be used to tailor various molding material properties, such as thermal conductivity and coefficient of thermal expansion, to meet module requirements. For example, these materials can include inorganic particles of glass, SiC,  $Al_2O_3$ , or AlN, particles of diamond or graphite, or metal particles of silver or copper. Glass, SiC, AlN, diamond, and graphite have low coefficients of thermal expansion, whereas polymers and metals have higher coefficients of thermal expansion. The thermally conductive materials include SiC, AlN, copper, graphite, and diamond, with graphite and diamond being the better conductors.

The substrate molding material is poured or injected into the mold form in a manner optimizing environmental conditions such as temperature, atmosphere, voltage, and pressure, to minimize voids, stresses, shrinkage and other potential defects. For example, the process works best when performed in a vacuum. Preferably, the processing temperature does not exceed 300 °C.

If the area of base sheet 12 is greater than the area of the mold form, a portion, depicted as removable section 300, of the base sheet can be trimmed before the base sheet is used in an HDI overlay structure (shown in FIGs. 1(d) and 1(e)). Alternatively, removable section 300 can be trimmed after module fabrication has been completed.

FIG. 1(c) is a sectional side view of the apparatus of FIG. 1(b) showing embedded chips after mold form 22 (shown in FIG. 1(b)) has been removed from molding material 24 and the base sheet 12 has been trimmed and separated from base 10. The substrate molding material is ready to be removed from the mold form after the molding material 24 is hardened (i.e., set with irradiation or cured at room temperature or with heat) into a molded substrate. Removal of the mold form can be facilitated if a release agent, such as Teflon polytetrafluoroethylene or vegetable oil, has been applied to the mold form. For epoxy molding material, a sprayed-on silicone mold release agent is preferred.

Base sheet 12 may be left in place on the surface of the molded substrate and the top surfaces of the IC chips and passive components. Typically adhesive layer 12a is a thermoplastic or thermoset material. Because the chips were placed face down before the molding process, the resulting surface of the molded substrate and chips is virtually planar, facilitating application of conventional HDI overlay structures (shown in FIG. 1(d)). This exposed surface can be treated with a short plasma  $O_2$  etch or RIE (reactive ion etch) exposure to promote adhesion during further processing.

ther processing.

In one embodiment, adhesive layer 12a is hardened before the molding material is added, and the molding material is hardened at a later time. In a preferred embodiment, the adhesive layer and the molding material are cured during a single heating step, thus reducing the number of processing steps. A single curing step works well if the adhesive layer and the molding material are fabricated of the same material, especially a thermosetting material.

Several examples of specific molding material and processing steps are discussed in the following paragraphs to describe potential specific molding techniques. The typical size of the mold is 2 inches long, 2 inches wide, and 50-60 mils high.

In a first example, a molding material is prepared by blending 50 g of SPI-135 solution (a siloxane-polyimide available from MicroSi Corp., Phoenix, AZ) with 50 g of a cycloaliphatic epoxy (CY-179, available from Ciba Geigy Corp.) which contains 1% by weight of an onium salt crosslinking catalyst, Octacat (available from GE Silicone Products, Waterford, NY). Other epoxy catalysts or co-catalysts, such as, for example, benzopinacol, copper naphthenate, and FC 520 (trifluoromethanesulfonic acid salt, available from 3M Corp.), can be used without sacrifice in performance or the ability to crosslink the molding material. This molding material is poured into the mold and baked for two hours at 100 °C under slight vacuum conditions to remove all solvents and bubbles. The mold is then heated for two hours at 130 °C followed by two hours at 180 °C to completely harden the molding material. These temperatures and times are for example only; they can be varied as desired. The preferred temperature range includes temperatures between 25 °C and 250 °C.

In a second example, a molding material is prepared by blending 50 g of Epon 828 (available from Shell Chemical), 50 g of D.E.N. 438, 5 g D.E.R. 732 (D.E.N. and D.E.R. available from DOW Chemical), 0.1 g of copper naphthenate blend from Mooney Chemical, and 1 g of Octacat crosslinking catalyst. The material is blended for one hour at 100 °C, poured into the mold form, heated for three hours at 130 °C, and then heated for five hours at 180 °C to harden the molding material.

In a third example, 50-200 g (typically 100 g) of finely powdered alumina (preferably particles having diameters less than 10 microns) is mixed with the blend of example two before the molding material is poured into the mold form. The mixture is heated as in example two, resulting in a composite molding material with improved thermal conductivity. Other materials such as aluminum nitride, aluminum silicon carbide, aluminum, or diamond particles can be blended and heated in a similar manner.

In a fourth example, molding material comprising 20 g of a siloxane polyimide polymer is dissolved in 80 g of Cy-179 (available from Ciba Geigy Corp.),

which is then blended with 0.8 g of Octacat and 0.1 g of copper naphthenate at 100 °C. The material is then combined, poured into a mold, and heated for three hours at 130 °C, followed by five hours of heating at 180 °C.

In a fifth example, an epoxy solution is prepared as described in the first example. A 1 mil thick Kapton polyimide film is surface-treated with an O<sub>2</sub> plasma reactive ion etch sequence to cause surface roughness and thus achieve improved adhesion. A portion of the epoxy solution is then spin coated on the Kapton polyimide film to result in a composite film of Kapton polyimide with a 1/2 mil thickness of the dried epoxy adhesive thereon. The film is baked at 100 °C for one hour to remove solvent and results in a 1/2 mil tack free film on one surface of the Kapton polyimide. The chips are placed face side down on the epoxy side of the film. The film is kept at about 100 °C, and some pressure is applied to the chips during placement to imbed the contact pads of the chips into the epoxy layer which is relatively soft at this temperature. Solvent die attach may be used for this purpose also, as described in aforementioned US-A-5,225,023. The mold form is placed around the chips and an additional portion of the epoxy solution (which has previously been heated to 100 °C to remove solvent) is poured hot over the backside of the chips, thus filling the mold. The entire structure is then heated for two hours at 130 °C and two hours at 180 °C to harden the mold material and the adhesive used to bond the chip to the Kapton polyimide (both of which comprise the epoxy solution).

Although using a thermoset adhesive layer, such as an epoxy, restricts rework processes, it is recommended for the dielectric layer adjacent to chips 14 because it permits lower HDI processing temperatures and allows for higher post fabrication processing and field application temperatures than thermoplastic adhesives.

FIG. 1(d) is a sectional side view of the apparatus of FIG. 1(c), further showing via openings 30 and a pattern of electrical conductors 32 which connect contact pads 15 on chips 14 and 20. Base sheet 12 forms the dielectric layer that, with electrical conductors 32, functions as a first interconnect layer 28 (FIG. 1(e)).

FIG. 1(e) is a sectional side view of the apparatus of FIG. 1(d), further showing a multi-layer HDI structure 26 situated on molded substrate 24 and including chips 20 and 14. HDI structure 26 includes first interconnect layer 28 comprising a dielectric layer with via openings 30 and supporting a pattern of electrical conductors 32, as well as an optional second interconnect layer 29 disposed over first interconnect layer 28. Additional interconnect layers could be applied, if desired. Methods of forming and filling via openings 30, methods of patterning electrical conductors 32, and methods of fabricating one or more upper inter-

connect layers 29 are described in Gorczyca et al., U.S. Pat. No. 5,161,093, issued Nov. 3, 1992, Eichelberger et al., U.S. Pat. No. 4,835,704, issued May 30, 1989, and Eichelberger et al., U.S. Patent No. 4,783,695, issued Nov. 8, 1988, each of which is commonly assigned and herein incorporated by reference.

FIGS. 2(a) and 2(b) are sectional side views of an alternative embodiment of the invention similar to that shown in FIGS. 1(a)-1(e). In this embodiment base sheet 12 (such as shown in FIG. 1(c)), which comprises a contact adhesive 12a coated on a polymer film 12b, is removed from the molded substrate 24 and chips 14 and 20. The base sheet is readily removed from the molded substrate if the adhesive film is selected for its low contact adhesion, such as, for example, wafer membranes of the types fabricated by Nitto Co. (known as "Nitto Tape") and Semiconductor Equipment Corp. (known as "Blue Membrane"). FIG. 2(a) is a view of molded substrate 24 and the chips supported thereon after removal of base sheet 12. FIG. 2(b) is a sectional side view of the apparatus of FIG. 2(a), further showing a dielectric layer 13 thereon comprised of an adhesive layer 13a and a polymer film 13b. This forms the first dielectric layer, and a structure similar to that illustrated in FIGS. 1(c)-1(e) can then be fabricated.

FIGS. 3(a)-3(d) are sectional side views of another alternative embodiment of the invention which is similar to that shown in FIGS. 1(a)-1(e). In this embodiment, however, base sheet 12 comprises an adhesive layer (such as Ultem polyetherimide resin) applied directly to base 10, as shown in FIG. 3(a), with no adjacent polymer film layer (such as layer 12b of FIG. 1(a)). Base 10, or the surface treatment of it, must be selected such that base sheet 12 will remain on molded substrate 24 after the base is removed. The substrate is molded with molding material 24, as shown in FIG. 3(b), in a manner similar to that for the apparatus of FIG. 1(b). FIG. 3(c) is a view similar to that of FIG. 3(b), showing the structure of FIG. 3(b) after removal of mold form 22 and base 10. FIG. 3(d) is a view similar to that of FIG. 3(c) further showing a polymer film layer 17 laminated to the molded substrate 24 through adhesive base sheet 12 by, for example, using heat and pressure or solvent and pressure. A preferred lamination technique is described in commonly assigned Eichelberger et al., U.S. Pat. No. 4,933,042, issued June 12, 1990, which is herein incorporated by reference. Film 17 may be pretreated with a plasma or RIE (reactive ion etching) for enhanced adhesion. A dielectric layer is thus formed on chips 14 and 20, and a method similar to that discussed with respect to FIGS. 1(c)-1(e) can be followed to fabricate an HDI structure.

FIG. 4(a)-4(c) and 4(e) are sectional side views of alternative embodiments of the invention which are similar to the views shown in FIGS. 1(a)-1(e). The

embodiment of FIG. 4(a) is similar to that of FIG. 1(a) except that it further includes an inner dielectric layer 100, such as, for example, an adhesive coated Kapton polyimide, overlying the backsides of chips 14. Dielectric layer 100 is applied to the chips prior to substrate molding material 24 (shown in FIG. 4(b)). The use of two chips, as opposed to five, is merely for simplicity of illustration; any number of chips can be used. Also, as shown in FIGs. 1(a)-3(d), the chips shown in FIGs. 4(a)-4(e) may have differing thicknesses.

The addition of inner dielectric layer 100 provides air gaps 102 between chips 14 and base sheet 12. These air gaps reduce stress on the module and relax the need for chips 14 and substrate molding material 24 to have a similar coefficient of thermal expansion. Another advantage of inner dielectric layer 100 is that a chip may be removed and replaced from an HDI structure using the convenient repair processes described in Wojnarowski et al., U.S. Patent No. 5,154,793, issued Oct. 13, 1992, and Eichelberger et al., U.S. Pat. No. 4,878,991, issued Nov. 7, 1989, which are commonly assigned and herein incorporated by reference. New chips may be replaced using an epoxy die attach material, preferably silver, and rebuilding the interconnections. Although not shown in the figures, inner dielectric layer 100 can also be used in the embodiments of FIGs. 2(a)-2(b), 3(a)-3(d), 5(a)-5(b), and 6(a)-6(b).

The embodiment of FIG. 4(c) further includes an electrically conductive strip, plate, or well, shown as strip 108, beneath inner dielectric layer 100. The strip comprises a ductile conductive material such as aluminum, gold, or copper, and in one embodiment has a thickness of four microns. One method for applying strip 108 to inner dielectric layer 100 is to place the inner dielectric layer on a support base and use the metallization and patterning processes described in aforementioned U.S. Patent No. 4,783,695. Strip 108 is positioned so that, when inner dielectric layer 100 is put down on the chips, one portion of strip 108 is in contact with the backside of a chip and another portion of strip 108 is on base sheet 12. Fine precision in placement of strip 108 is not required; the strip is effective so long as it touches any portion of a chip and any portion of the base sheet. Preferably either the backside of the chip or the strip is coated with silver epoxy die attach material (not shown) to improve electrical contact.

FIG. 4(d) is a top view of the structure of FIG. 4(c), showing the location of conductive strip 108 relative to one of chips 14. This strip may be used, for example, to ground the chip to which it makes contact, or to supply a desired voltage to the chip.

As shown in FIG. 4(e), at least one via 30 is fabricated through base sheet 12 to allow contact to a chip pad. At the same time vias 30 are fabricated, a via 110 may be drilled through base sheet 12 to strip

108. An electrically conductive strip connection 106 to ground or a voltage source may be fabricated simultaneously with the pattern of electrical conductors 32 that are electrically connected to chip pads through vias 30.

FIG. 5(a) is a sectional side view of an embodiment of the invention similar to that shown in FIG. 1(a), further including thermal or thermo-electrical plugs, shown as thermal plugs 34, situated on passive backsides of chips 14. These plugs can be bonded to the chips by silver epoxy (not shown) for grounding purposes, if desired. The thermal conductivity required varies according to thermal dissipation characteristics of the module, environmental conditions of the planned application, and the projected life of the circuit. High thermal conductivity filler material, such as graphite, silver epoxy, or diamond, is sufficient for most high power applications. Thermal plugs 34 are useful for extremely high power densities, such as those exceeding 100 watts per module. If desired, an inner dielectric layer, such as layer 100 shown in FIGs. 4(a)-4(e), can be placed over chips 14 prior to the addition of thermal plugs 34. Preferably, such inner dielectric layer would be ablated or thinned in the area where the thermal plugs are desired before the thermal plugs are placed on the chips.

Thermal plugs 34 may comprise any thermally conductive material, including, for example, molybdenum or copper or a mixture, such as a silicon carbide matrix infiltrated with aluminum, as fabricated by Lanxide Corporation. Preferably the thermal plug both provides the necessary dissipation and has a coefficient of thermal expansion selected so as not to differ greatly from that of the chips. The thermal plugs can be attached to the backs of the chips following the step of attaching the chips to base sheet 12 but prior to the step of adding the molding material 24, which is shown in FIG. 5(b), using an epoxy attach material that may have a cure temperature ranging from room temperature to elevated temperatures insufficiently high to damage chips 14 and 20. Preferably the thicknesses of thermal plugs 34 are such that the surfaces opposite the surfaces attached to chips 14 are positioned on a common plane. This can be achieved by using appropriately thinner thermal plugs on thicker chips.

FIG. 5(b) is a sectional side view similar to that of FIG. 5(a), further showing mold form 22 situated around the chips and thermal plugs and filled with molding material 24. In the illustrated embodiment, the height of mold form 22 does not exceed that of the thermal plugs attached to the chips. Preferably thermal plugs 34 and mold form 22 are selected so that the resultant substrate and outer edges of the thermal plugs will be coplanar. Alternatively, common height thermal plugs may be used and, following hardening of the molding material, be mechanically or chemically planarized. The thermal plugs can provide a high

thermal conduction path directly to a heat sink (not shown). Although not shown in FIG. 5(b), the thermal plugs may extend beyond the mold surface for enhanced heat sink attachment or for mounting.

An HDI substrate molded in accordance with the above-described embodiments can either be a drop-in substrate which is mounted in an enclosure for protection from the environment or a stand-alone component that is either directly mounted onto a board or utilized as a free standing module. The drop-in version can have external connections from the outermost interconnect layer of the HDI structure, such as layer 29 shown in FIG. 1(e).

In free standing modules, electrical interconnections from the HDI multi-chip module (MCM) can be made in a number of variations. Like the drop-in version, the interconnections can be made from the outermost interconnect layer of the HDI structure. This outermost interconnect layer can include area contact pads comprised of Ti:Cu:Ti:TiW:Cu, for example. Gold is beneficial as the outermost connecting material because it is highly conductive and will not corrode. Alternatively, interconnect material may comprise Ti:Cu for connection by a solder attach process.

Another embodiment of the invention uses an interconnect structure molded into the substrate. One variation of this concept involves placement of a connector frame 39 (FIGs. 6(a) and 6(b)) around the chips prior to the molding step. The frame can provide connection pads coplanar with the chip faces. Thus FIG. 6(a), which is a sectional side view similar to that of FIG. 1(d), further shows a perimeter array of interconnect pins 36 having connection pads 37 in base sheet 12. Pins 36 extend through the surface of substrate 24 opposite the surface of base sheet 12 to which chips 14 and 20 are attached. These pins may be designed to be compatible with any connectors with which the pins will interface. For example, the pins can be fabricated for use with pin grid array sockets. A dielectric layer 40 can be used to cover and protect the pattern of electrical conductors 32.

FIG. 6(b) is a view similar to that of FIG. 6(a), except that the perimeter array of interconnect pins 38 extends through a side of substrate 24. This embodiment is useful for lower pin count modules, such as those applicable to automotive electronics. There are several methods for designing the side extensions. The mold form can have openings in the side which allow for placement of the connector frame. Alternatively, the pins, which are sufficiently longer than the molding material thickness, may be bent toward the side after the mold is cured or set. A dielectric layer, such as dielectric layer 100 shown in FIGs. 4(a)-4(e), can be placed over chips 14 prior to the addition of substrate material 24. Such dielectric layer has to be ablated in the area where the connectors (36 in FIG. 6(a) or 38 in FIG. 6(b)) will be placed.

Large arrays of substrates can be fabricated as

on large wafers that can be readily cut apart either before or after the HDI fabrication is completed, thus reducing handling.

FIG. 7(a)-7(d) are sectional side views of several alternative embodiments of the invention shown in FIGs. 1(a)-1(e). In these embodiments, there is no base sheet 12 (FIG. 1(a)), and a vacuum plate is used as base 10.

In one embodiment, chips 14 are placed face down on base 10 comprising a vacuum plate, as shown in FIG. 7(a). The vacuum plate, which may comprise any appropriate structural material, is typically porous and may be coated with a mold release material (not shown), such as Teflon polytetrafluoroethylene, silicone, or a no-stick vegetable oil, for ease of removing hardened substrate molding material. Any orifices which are not covered by chips 14 are preferably masked so that the subsequently applied substrate molding material does not enter the vacuum plate. One mask technique is to apply a material such as Teflon polytetrafluoroethylene tape or thin silicone rubber sheets over any exposed orifices.

A continuous vacuum is applied to the vacuum plate throughout chip placement. The substrate is molded with molding material 24, as shown in FIG. 7(b), in a manner similar to that discussed with respect to FIG. 1(b). Chip pads 15 are preferably short enough so that molding material 24 does not flow under the chips. When a mold release material is on the vacuum plate and the chip pads are pressed into the release material, molding material is further prevented from flowing under the chips. FIG. 7(c) is a view similar to that of FIG. 7(b), further showing embedded chips in substrate molding material after the vacuum plate and the mold form have been removed. Then a dielectric layer, such as layer 13 shown and described with reference to FIG. 2(b), can be applied and an HDI structure can be fabricated by the steps discussed with respect to 1(c)-1(e).

FIG. 7(d) illustrates another embodiment in which a vacuum plate is used. Base 10 is a rigid vacuum plate comprising a material such as stainless steel. The chips are positioned while a continuous vacuum is applied to the rigid vacuum plate. Then the chip locations are monitored and modified, if desired. The vacuum conditions remain while a second, non-compliant vacuum plate is pressed onto the top surface of the chips, which can be non-planar. As shown in FIG. 7(e), the compliant vacuum plate envelops the chips. Preferably this compliant vacuum plate comprises two layers: one compliant layer 710 of material such as silicone rubber and one firm support layer 712 such as stainless steel. After the compliant vacuum plate is pressed around the chips, a continuous vacuum is applied to the compliant vacuum plate. The vacuum is then released from the rigid vacuum plate, and the rigid vacuum plate is removed.



After the rigid vacuum plate is removed, the compliant vacuum plate is inverted while the chips remain on the compliant vacuum plate but are no longer pressed into the compliant vacuum plate. As shown in FIG. 7(f), the chips are in a similar position as the chips shown in FIG. 7(a). The remainder of steps in the HDI fabrication process are those discussed with respect to FIGs. 7(a)-7(c).

If desired, an inner dielectric layer 100, as discussed with respect to FIGs. 4(a)-4(e), thermal plugs 34, as discussed with respect to FIGs. 5(a)-5(b), a connector frame 39, as discussed with respect to FIGs. 6(a)-6(b), or any combination of these features can be used in the embodiments disclosed with respect to FIGs. 7(a)-7(f). The only difference would be that an inner dielectric layer or a connector frame would be applied on a vacuum plate instead of on a base sheet.

FIGs. 8(a)-8(e) are sectional side views of alternative embodiments of the invention which are similar to the views shown in FIGs. 1(a)-1(e). The embodiment in FIG. 8(a) is similar to a partial view of FIG. 1(b) except that substrate 24 has been inverted and a mechanical grinding fixture 810 has been provided. The mechanical grinding fixture is used to grind down the backside of the substrate to a desired thickness, which may be to the bottom surface of a chip 14, part way through the chip, or to a thickness somewhat greater than the chip thickness. Thinning a substrate saves space and lowers thermal resistance.

During the grinding, the substrate molding material surrounding the chips holds the chips in place and helps protect the chips from chipping or cracking. This process is not limited to mechanical grinding; other techniques are available for removing substrate material and thinning the structure, such as, for example, chemically dissolving the selected portion of the substrate molding material. Commonly assigned Wojnarowski, "Thinning of Integrated Circuit Chips for Lightweight Packaged Electronic Systems and Systems Produced Therefrom," Application Ser. No. 07/962,379, filed Oct. 16, 1992, discloses additional thinning options such as ultrasonic milling, micro blasting, milling, laser cutting, and using a lapping machine, and is herein incorporated by reference.

After substrate 24 is thinned, it appears as shown in FIG. 8(b). Then base 10 is removed, and an integrated circuit module (shown as HDI structure 859), similar to that discussed with respect to the embodiment of FIGs. 1(c)-1(e), can be fabricated, as shown in FIG. 8(c) where upper interconnect layers 812 and 814 overlie polymer film layer 12b and chips 14 are interconnected by a pattern of electrical conductors 32. The substrate thinning process can be used in combination with any of the techniques discussed with respect to the embodiments of FIGs. 1(a)-7(f), except that chips would preferably not be thinned in

the embodiments of FIGs. 4(a)-4(e) and, because of the lower thermal resistance of thinned structures, thermal plugs 34 (FIGs. 5(a)-5(b)) are not as necessary as the plugs might be in thicker structures.

These HDI structures can be stacked, as shown in the embodiment of FIG. 8(d). In one type of stacking, edge metallization contacts 852 are used. Methods for fabricating these contacts are disclosed in Eichberger et al., U.S. Pat. No. 5,019,946, issued May 28, 1991, and Gorczyca et al., "Edge-Metallized High Density Interconnect Substrates to Enable Fabrication and Interconnection of Three-Dimensional Modules," Application Ser. No. 07/959,886, filed Oct. 13, 1992, both of which are commonly assigned and incorporated herein by reference.

HDI structure 859 of FIG. 8(d) is coated with an adhesive layer 816 so that at least one additional HDI structure 860 can be attached. HDI structure 860 is provided with thinned chips 820 in thinned substrate 818. An adhesive layer 821 is positioned between the top face of thinned substrate 818 and a dielectric layer 822 having a pattern of electrical conductors 828 with edge contact pads 852 for interconnecting the chips. More interconnections can be provided by an optional additional dielectric layer 824. Dielectric layer 826 is useful as a buffer between HDI structure 860 and another HDI structure 862.

HDI structure 862 is stacked on a top surface, shown as dielectric layer 826 of HDI structure 860. An adhesive layer 830 bonds the bottom surface of HDI structure 862 to the top surface of HDI structure 860. High density interconnect structure 862 is provided with thinned chips 832 in thinned substrate 834. An adhesive layer 836 is positioned between the top face of thinned substrate 834 and a dielectric layer 838 having a pattern of electrical conductors 844 with edge contact pads 852 for interconnecting the chips. More interconnections can be provided by an optional additional dielectric layer 840. Dielectric layer 842 is useful as a buffer for HDI structure 862.

An edge dielectric layer 846 is applied to a side of the stack having edge contact pads by an adhesive (not shown) and vias 854 are formed over selected edge pads. Then a conductive metal track structure 848, positioned on the exposed side of dielectric layer 846, electrically connects, through the vias, at least some of the edge contact pads.

FIG. 8(e) illustrates an alternative method of stack assembly and interconnect. In this embodiment the stacks are formed in a similar manner as previously described, except that instead of using edge contact pads 852 (FIG. 8(d)) an array of substrate pins 850 is molded into each plastic substrate during the initial molding process. Pin contact pads 856 can be deposited onto the top and bottom pin surfaces by applying and patterning a metal such as gold.

Area input/output (I/O) contacts 858 such as, for example, fuz buttons, elastomers, and solder

bumps, are located at the pad sites to interconnect the HDI structures. Fuzz buttons are typically round balls of fine electrically conductive fibers. One method of applying them is to place a spacer layer (not shown) having holes above selected portions of the pattern of electrical conductors. Fuzz pads can then be inserted into the holes, and the next HDI structure can be applied. Conductive elastomer contacts can be fabricated by using a sheet (not shown) having vertically aligned contacts which touch when squeezed together. The sheet is positioned on a top surface of an HDI structure so that the vertical contacts are situated above selected portions of the pattern of electrical conductors. Then an HDI structure is applied. With both elastomer contacts and fuzz buttons, it is useful to have a clamp (not shown) or some other means for pressing the HDI structures together. Additionally, silicone epoxy can be used near the I/O interfaces during clamping for securing the structures after a clamp is removed. A spacer is also useful for solder bumps. In this case, no clamp is needed because the bumps are heated to form connections.

Interconnection from the stacked module to the next level of packaging can be made from either the top pads or the bottom pads, as required. The thin profile and the excellent thermal path permits many more levels in the stack than are available in a conventional HDI stack.

While only certain preferred features of the invention have been illustrated and described herein, many modifications and changes will occur to those skilled in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes.

#### Claims

1. An integrated circuit module, comprising:
  - a plurality of chips, each of said chips having contact pads located on a common plane;
  - hardened substrate molding material surrounding said chips, except for the faces of said chips;
  - a dielectric layer situated on the faces of said chips and said hardened substrate molding material, said dielectric layer including a plurality of vias therein, at least some of said plurality of vias being aligned with predetermined ones of said contact pads, respectively; and
  - a pattern of electrical conductors extending through selected ones of said plurality of vias in said dielectric layer.
2. The module of claim 1, wherein said hardened substrate molding material comprises plastic.
3. The module of claim 2, wherein said hardened

substrate molding material comprises material selected from the group consisting of thermoplastics, thermosets, polyetherimides, polytetrafluoroethylenes, epoxies, benzocyclobutene, acrylates, polyurethanes, and polyimides.

4. The module of claim 2, wherein said hardened substrate molding material includes filler material therein selected from the group consisting of glass, SiC, Al<sub>2</sub>O<sub>3</sub>, AlN, diamond, graphite, and metal.
5. The module of claim 4, wherein said filler material is in one of the configurations selected from the group consisting of particles, fibers, screens, mats, and plates.
6. The module of claim 1, wherein said dielectric layer comprises a thermoset material.
7. The module of claim 6, wherein said hardened substrate molding material comprises a thermoset material.
8. The module of claim 1, wherein said substrate molding material comprises a blend of polyimide, epoxy, and crosslinking catalyst.
9. The module of claim 8, wherein said substrate molding material further comprises particles selected from the group consisting of alumina, aluminum nitride, aluminum silicon carbide, aluminum, and diamond.
10. The module of claim 8, further including an adhesive layer between said dielectric layer on one side and said chips and said substrate molding material on the other side, and wherein said adhesive layer comprises the same material as said substrate molding material.
11. The module of claim 1, further including a thermal plug extending from the backside of at least one of said chips at least through to the opposite side of said hardened substrate molding material.
12. The module of claim 11, wherein said thermal plug comprises an electrically conductive material.
13. The module of claim 11, wherein said thermal plug comprises a material selected from the group consisting of copper, molybdenum, and a silicon carbide matrix infiltrated with aluminum.
14. The module of claim 1, further including a connector frame including contact pads coplanar

with contact pads around said chips positioned in said hardened substrate molding material.

15. The module of claim 14, wherein said connector frame further comprises an array of pins which extend at least through said substrate molding material to the surface thereof. 5
16. The module of claim 14, wherein said connector frame further comprises an array of pins which extend at least through to the side of said substrate molding material. 10
17. The module of claim 1, further including an inner dielectric layer positioned between said chips and said hardened substrate molding material. 15
18. The module of claim 17, further including an electrically conductive strip extending along said inner dielectric layer from the backside of at least one of said chips to said dielectric layer. 20
19. The module of claim 18, further including an electrical connection from said electrically conductive strip to one potential selected from the group consisting of a voltage source and ground. 25
20. The module of claim 1, further including:  
an additional dielectric layer situated over said dielectric layer, said additional dielectric layer including a plurality of additional vias therein, at least some of said plurality of additional vias being aligned with predetermined portions of said pattern of electrical conductors; and  
an additional pattern of electrical conductors extending through selected ones of said plurality of additional vias in said additional dielectric layer. 30 35

40

45

50

55

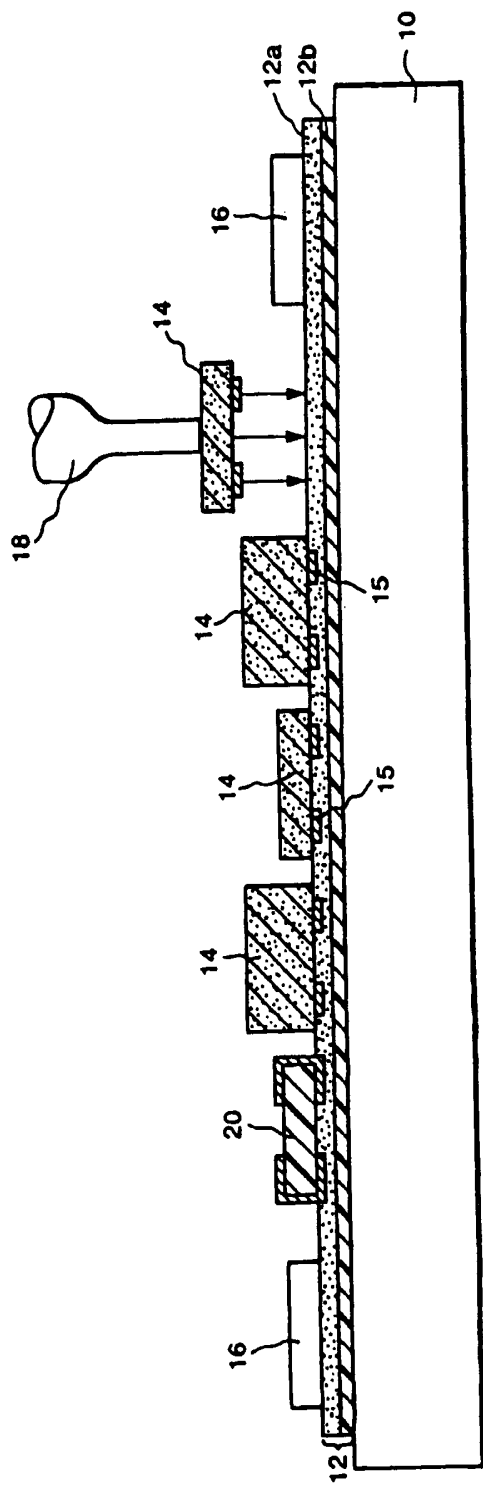


FIG. 1(a)

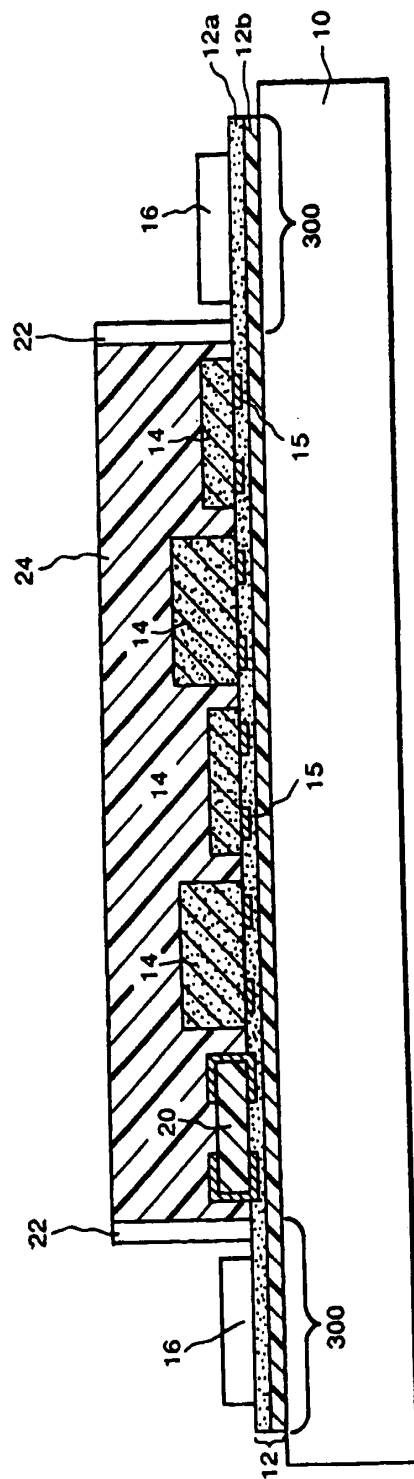


FIG. 1(b)

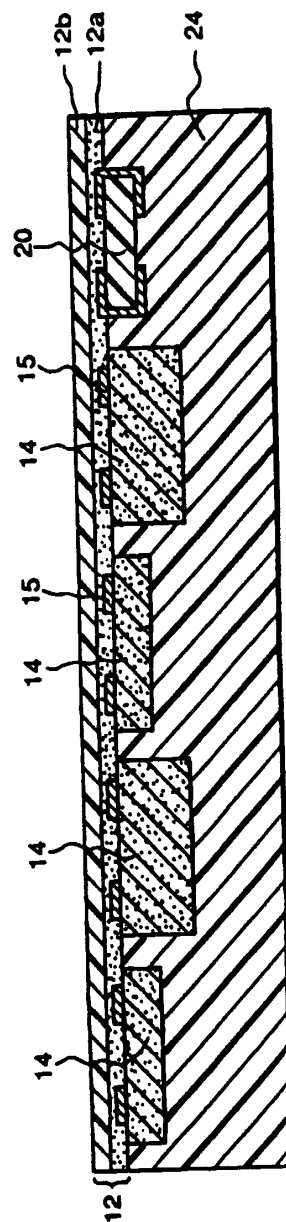


FIG. 1(c)

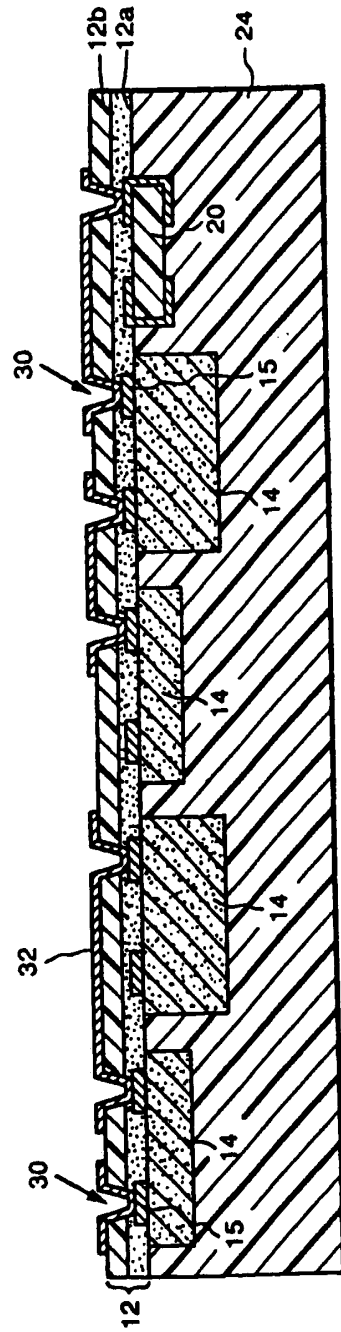


FIG. 1(d)

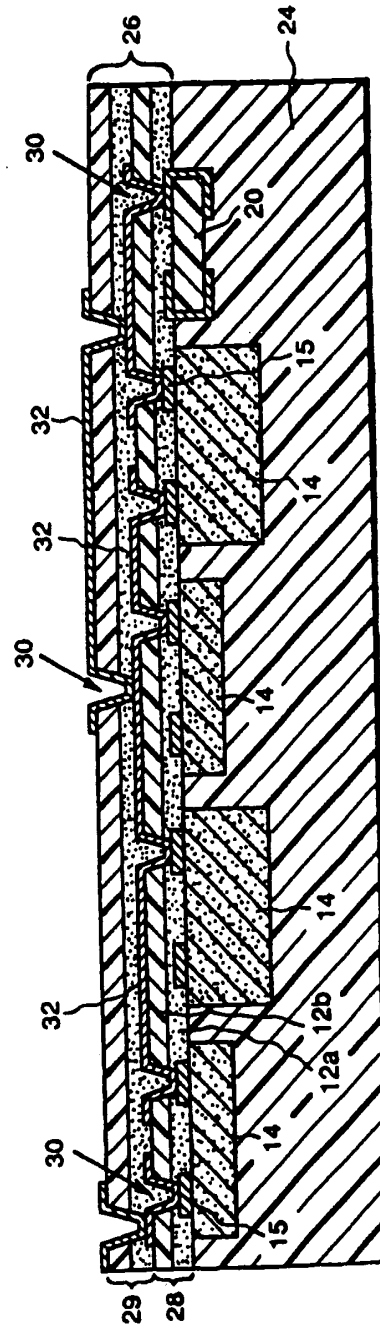


FIG. 1(e)

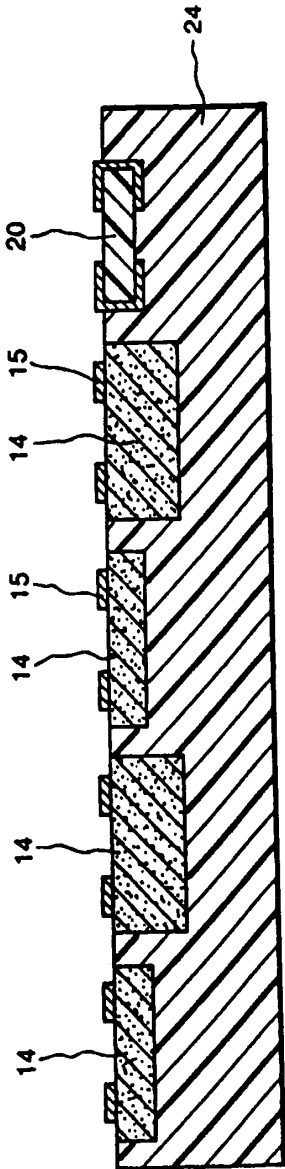


FIG. 2(a)

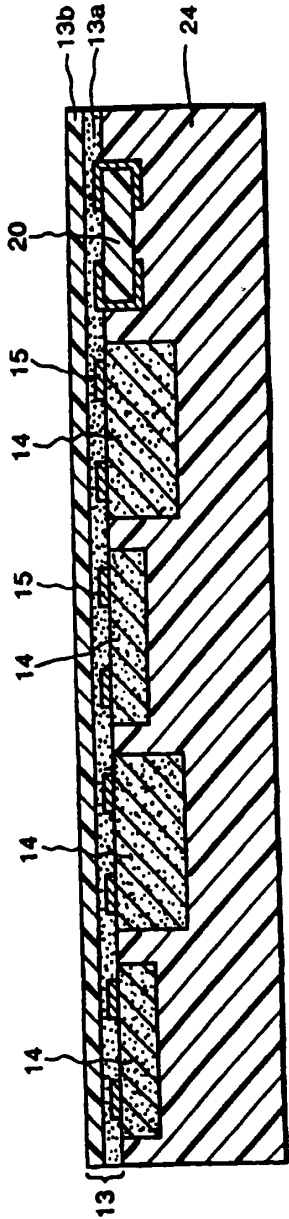


FIG. 2(b)

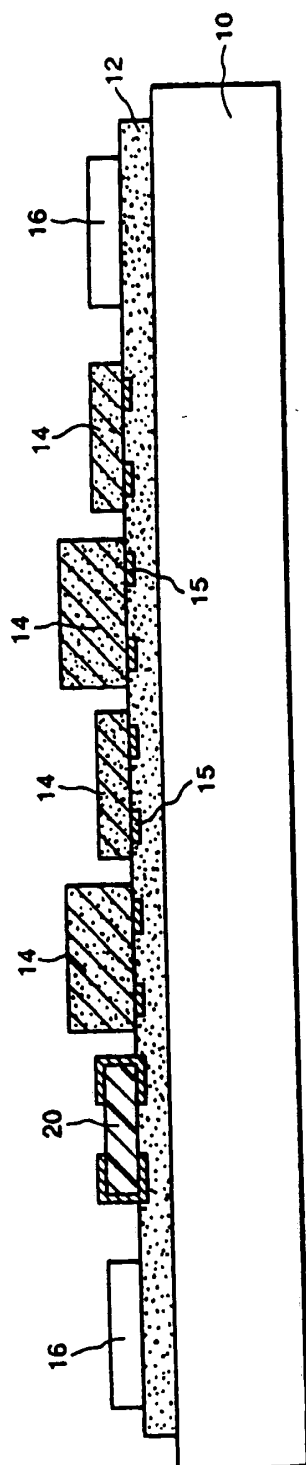


FIG. 3(a)

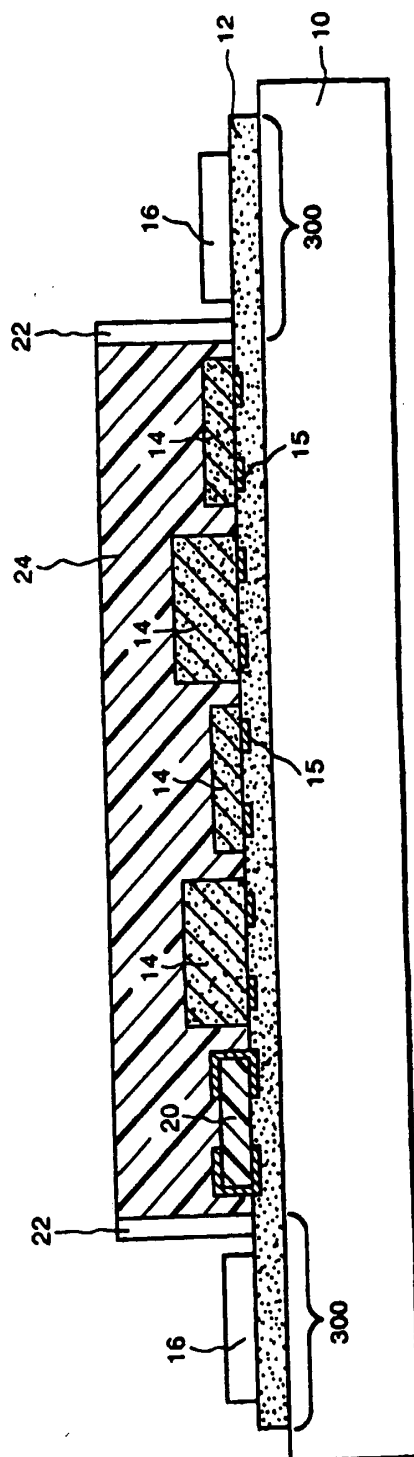


FIG. 3(b)



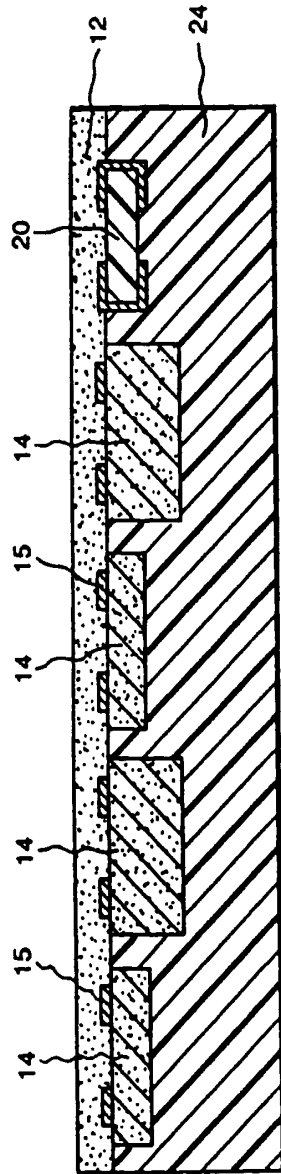


FIG. 3(c)

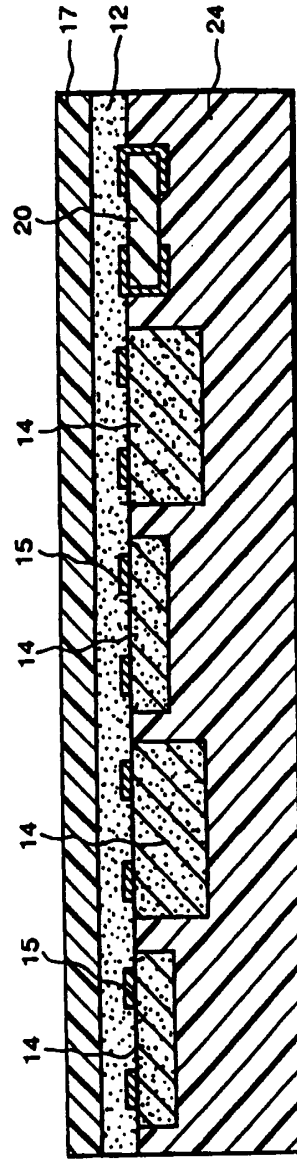


FIG. 3(d)

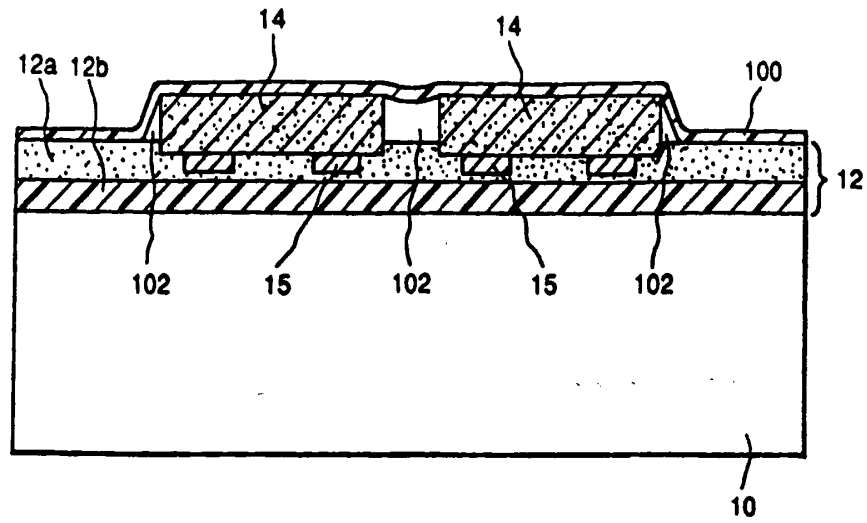


FIG. 4(a)

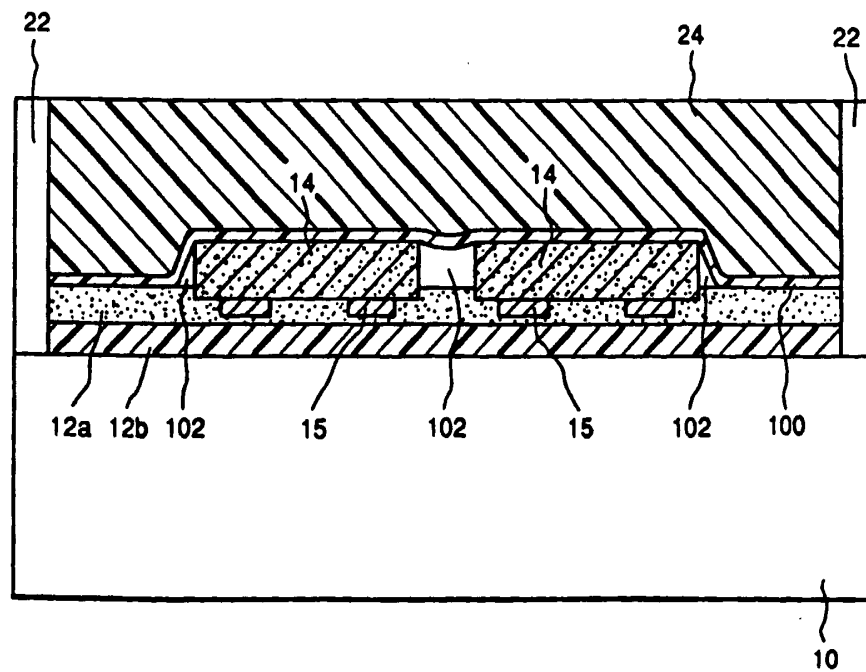


FIG. 4(b)

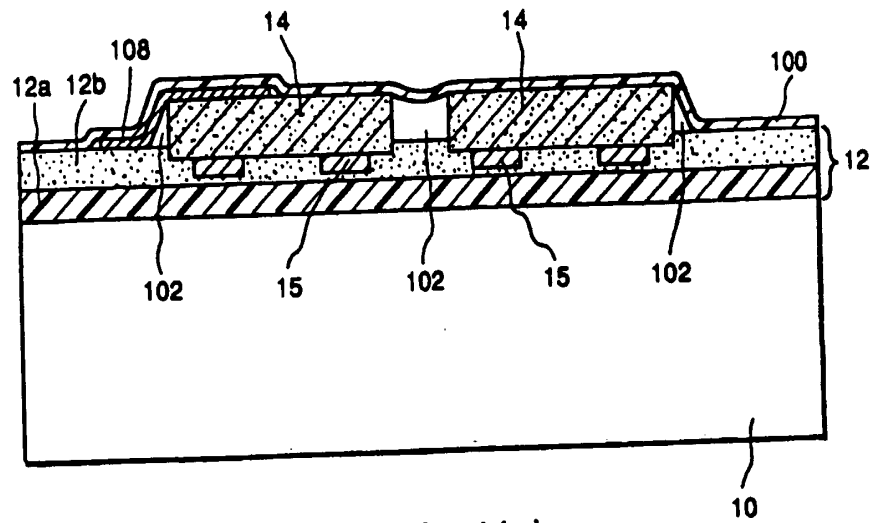


FIG. 4(c)

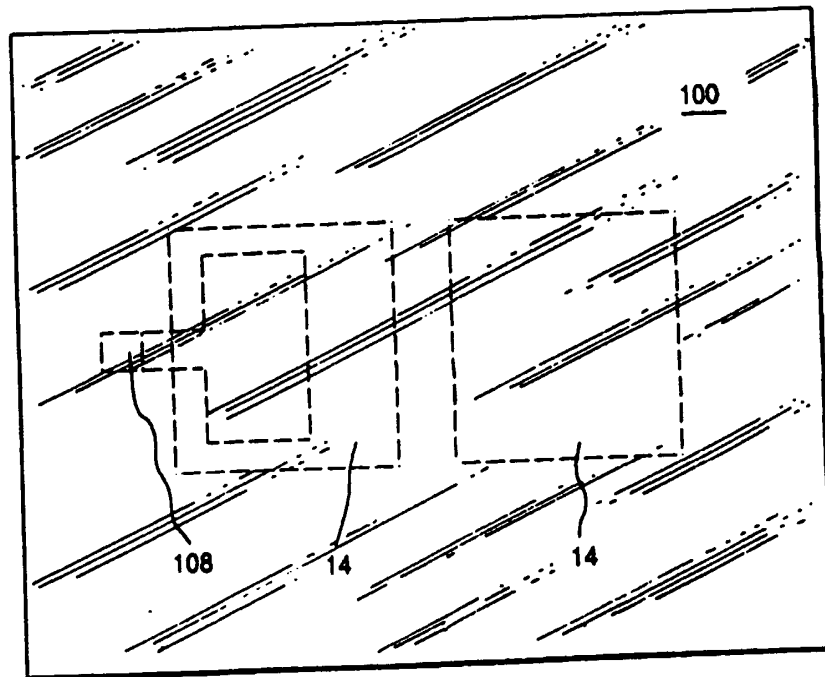


FIG. 4(d)

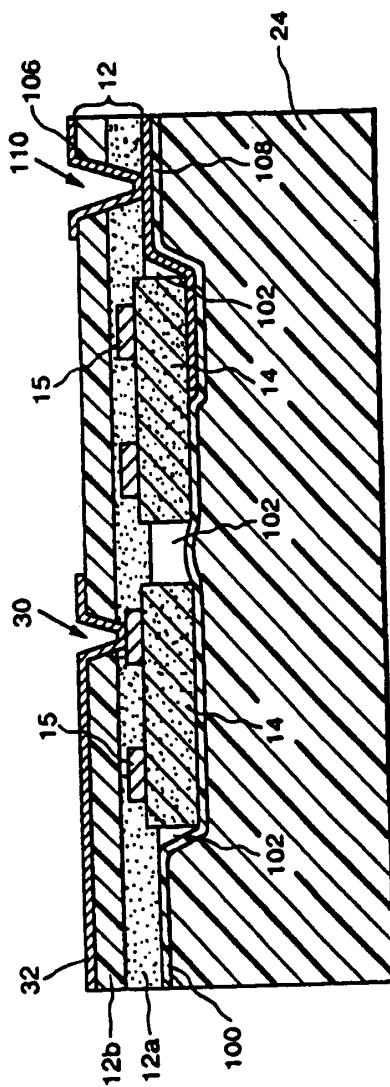


FIG. 4(e)

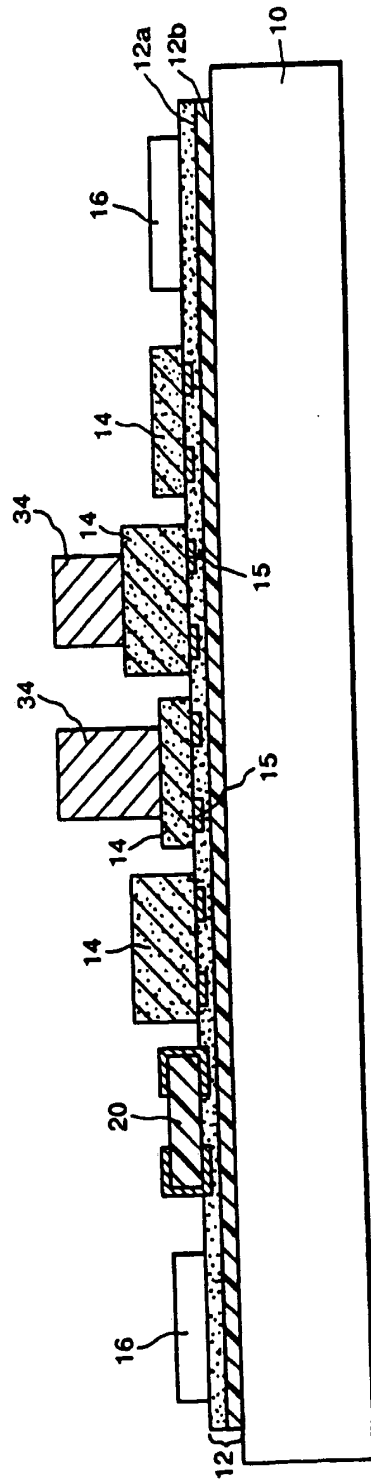


FIG. 5(a)

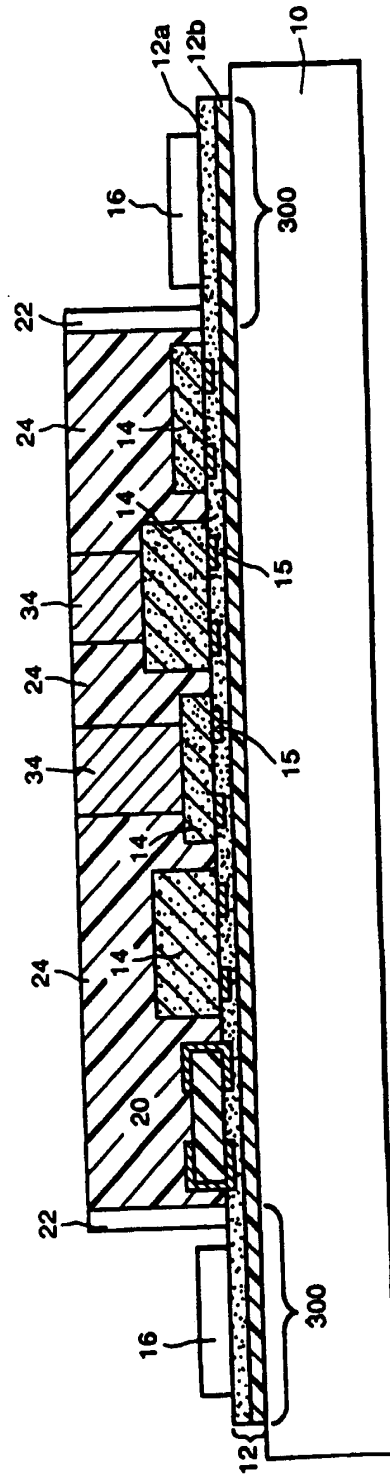


FIG. 5(b)

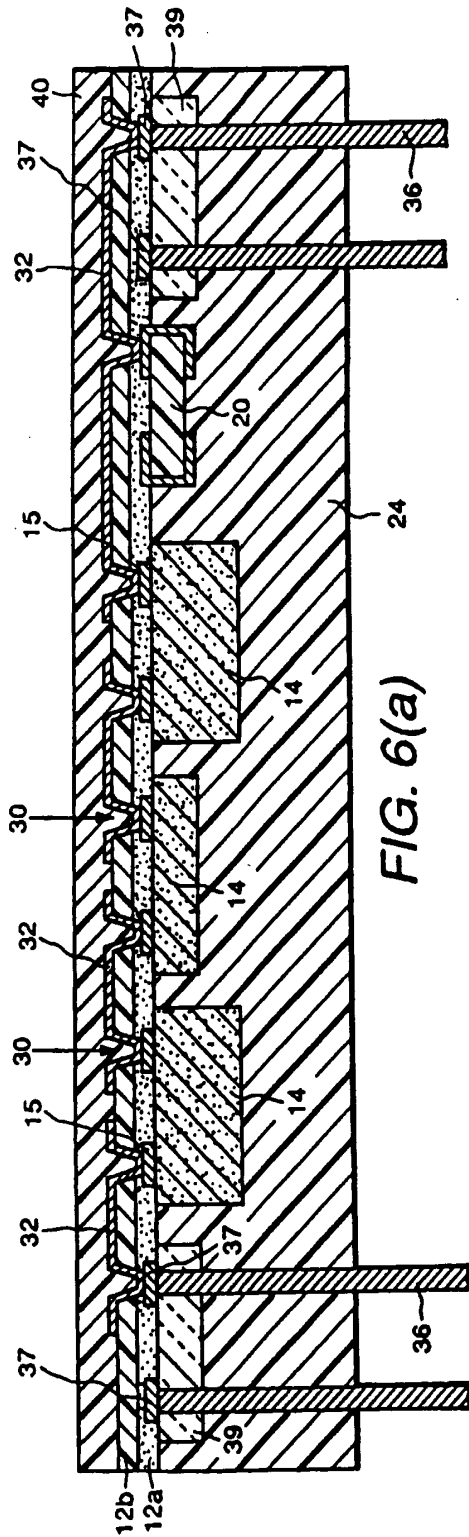


FIG. 6(a)

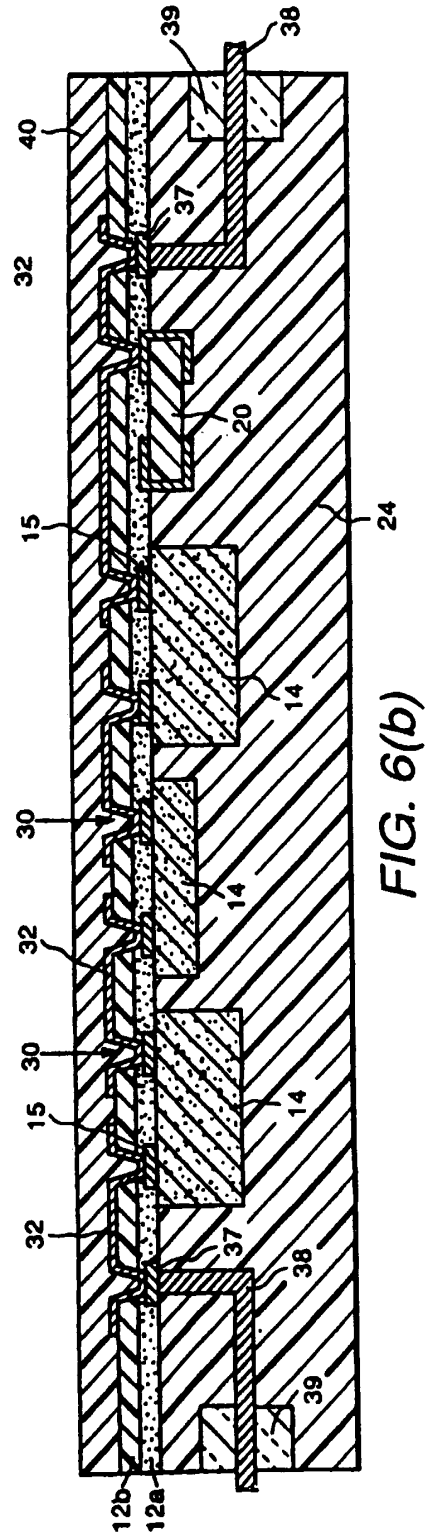


FIG. 6(b)

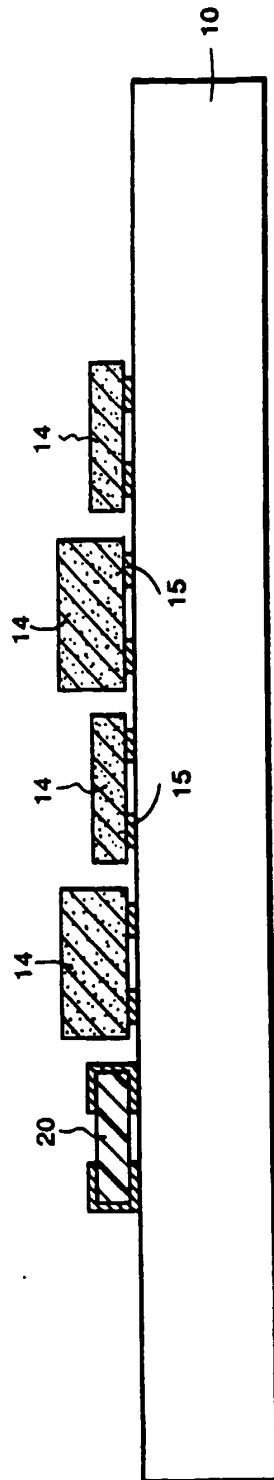


FIG. 7(a)

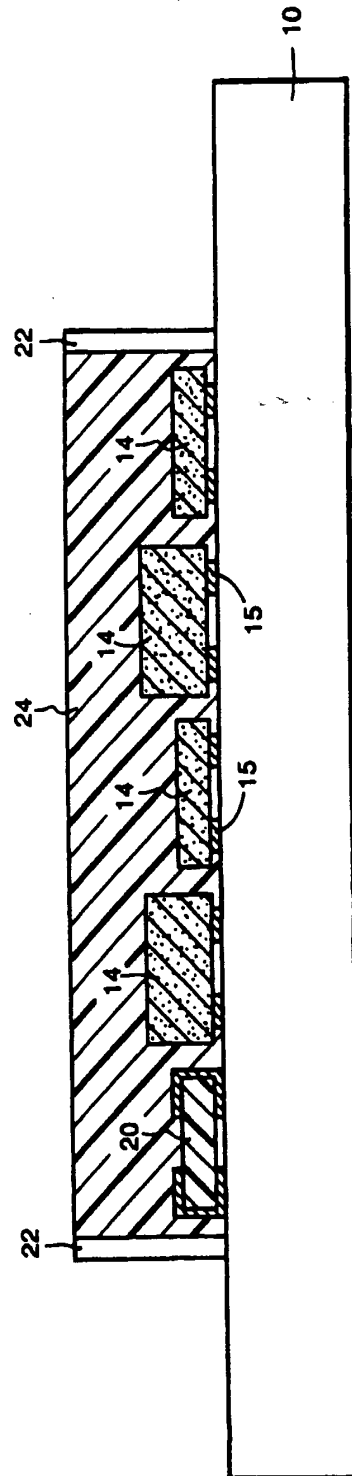
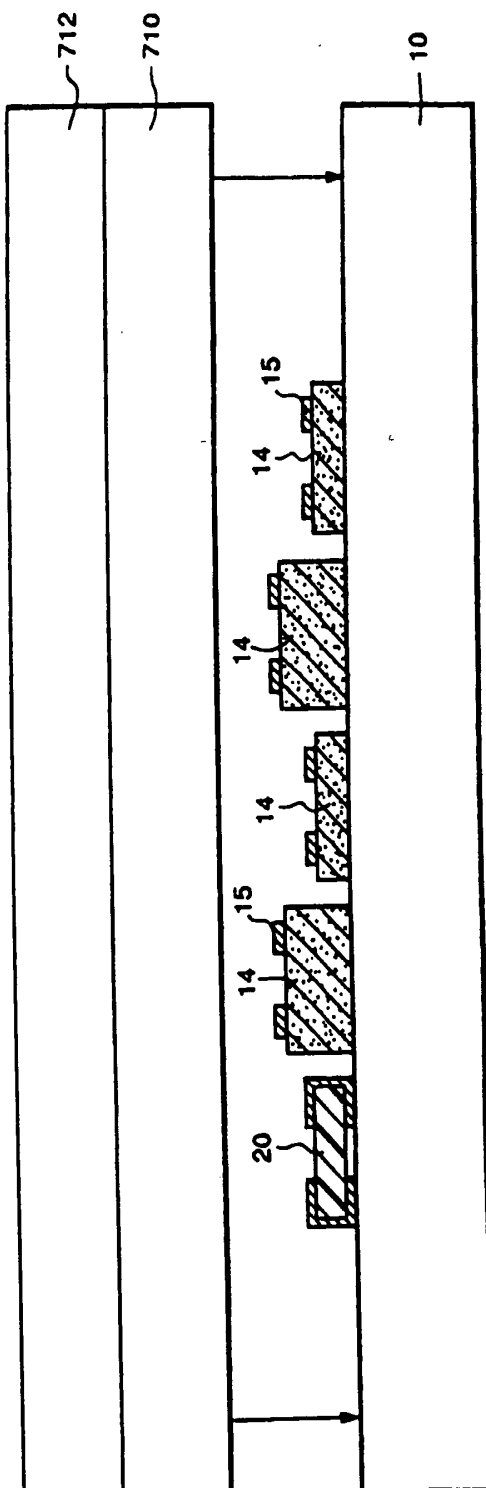
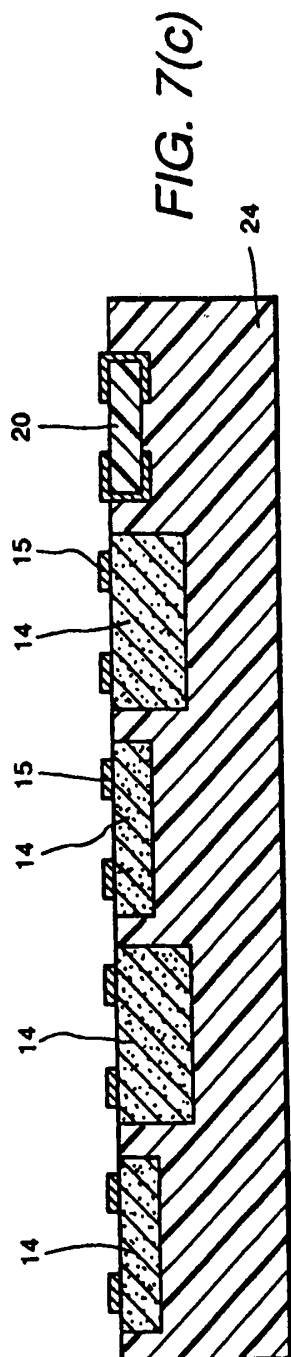


FIG. 7(b)





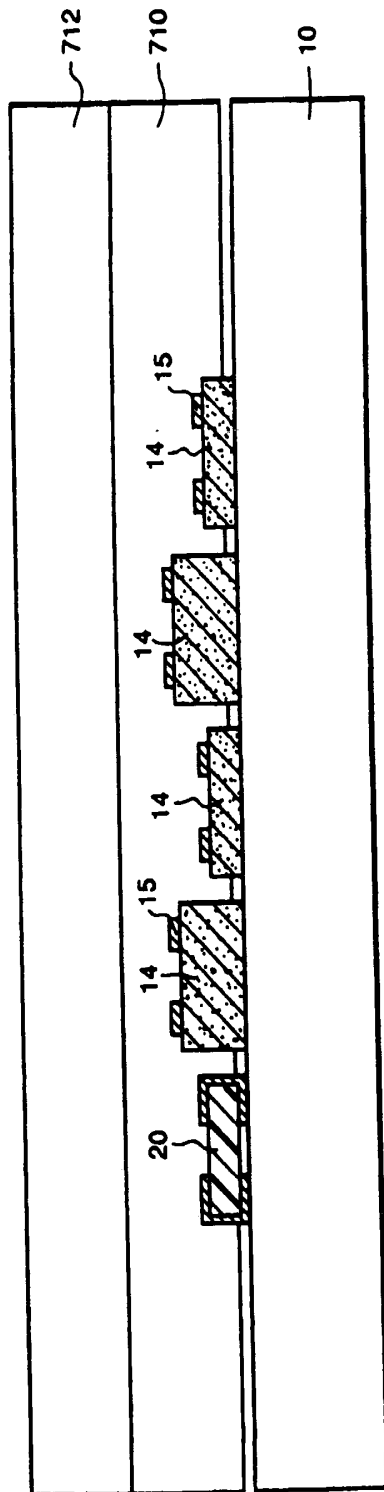


FIG. 7(e)

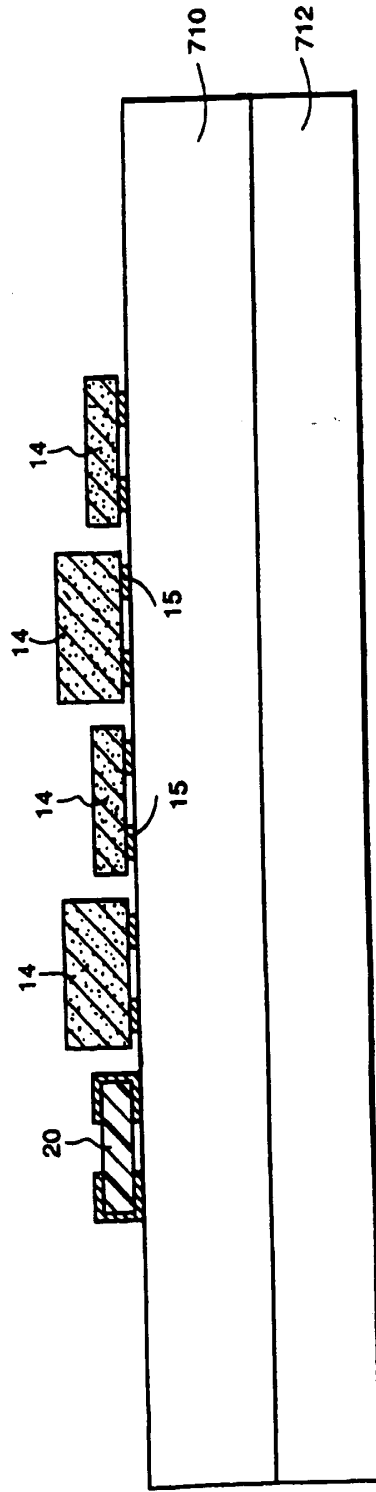
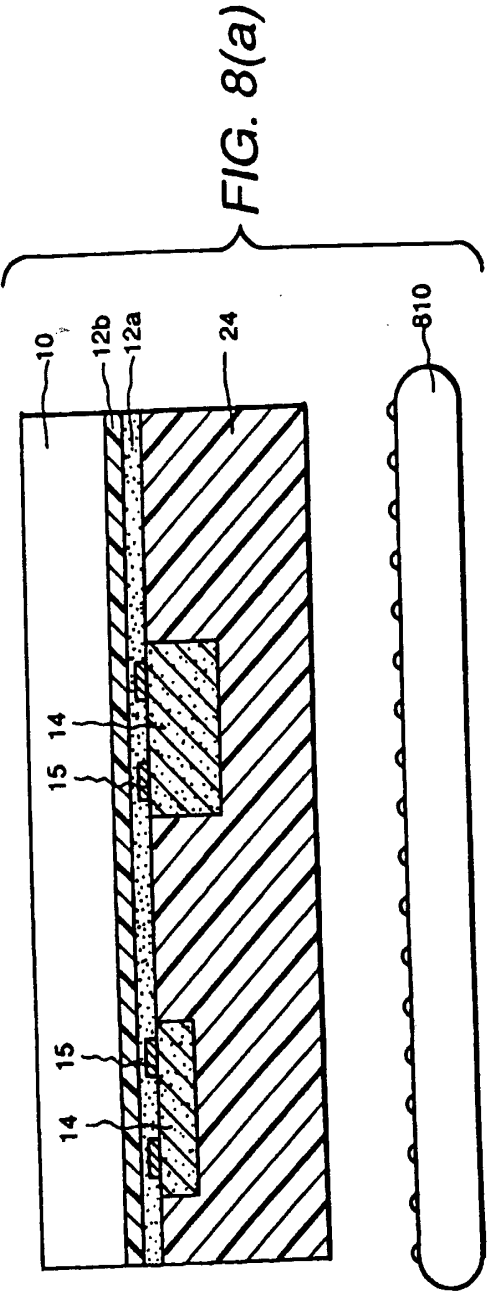


FIG. 7(f)



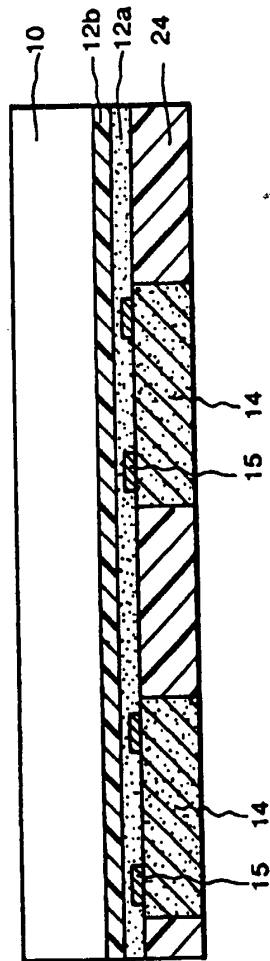


FIG. 8(b)

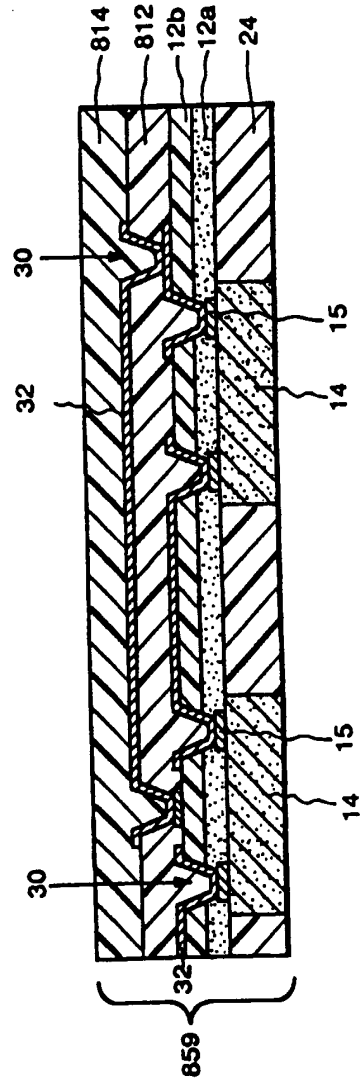


FIG. 8(c)

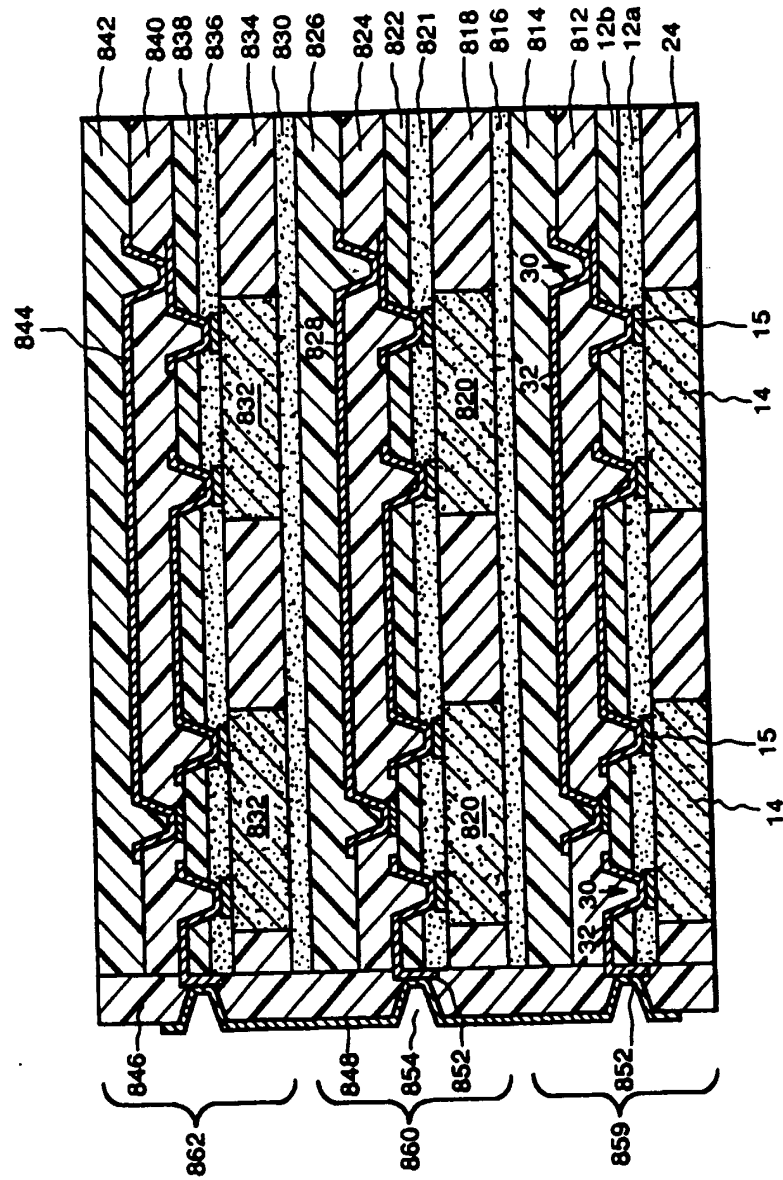


FIG. 8(d)

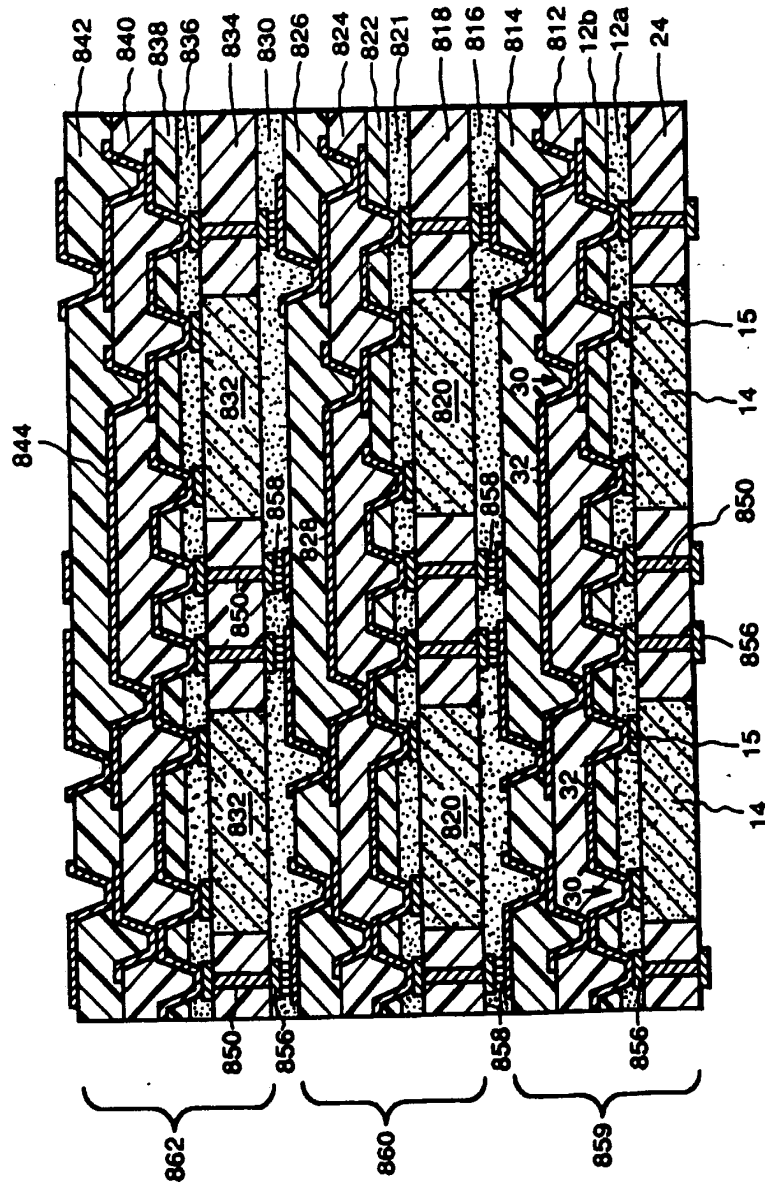


FIG. 8(e)